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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/565,618	ZINGHER, ARTHUR R.	
	Examiner	Art Unit	
	DAVID J. HUISMAN	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 19-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 19-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2006 & 20 May 2010* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 and 19-31 have been examined.

Comments

2. Applicant's amendments to not comply with 37 CFR 1.121, which requires that deletions not denoted by strike-through must be denoted by double brackets, not single brackets. Failure to comply with 37 CFR 1.121 in future submissions may result in the issuance of a notice of non-compliance.

Drawings

3. The drawings are objected to because:

- in Figs.1, 2, 4, and 6, the text size is too small. All text must be at least 1/8 inches in height. See 37 CFR 1.84(p)(3).
- In Fig.4, the upside down text should be flipped so that it is readable in the default upright view. It would still be readable when turned to the side view as well.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the

drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Throughout the claims, applicant is inconsistent with the use of dashes. Specifically, applicant claims "fast-response" and "fast response" throughout the claims. Please ensure that dashes are used consistently.

5. In claim 27:

- insert a dash between "time" and "distortion".
- what does 3x mean? Please write in words what this stands for.
- also, applicant should clarify what is meant by "less than 3x". What X occurs with respect to Y at a ratio less than 3 to 1?

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 25-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. The phrase "substantially unchanged" in claim 25 is a relative term which renders the claim indefinite. The phrase "substantially unchanged" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. What does it mean to be substantially unchanged?

9. The phrase "substantially simultaneously" in claim 26 is a relative term which renders the claim indefinite. The phrase "substantially simultaneously" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. What does it mean to occur substantially simultaneously?

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-4, 6-10, 19-22, and 25-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Takahashi, U.S. Patent No. 4,755,997 (submitted as part of the international search report filed on January 24, 2006, by applicant).

12. Referring to claim 1, Takahashi has taught a debugging system, comprising:

a) an integrated circuit chip comprising a processor constructed to execute a program and to generate results data. See Fig.4, component 4a. Processors inherently execute programs to generate results.

b) a data path constructed to transfer data from the processor. See Fig.4 and note the data path coupling the processor 4a to components 4c-e, 4g-h, and 21-23. This data path carries data from the processor.

c) a fast-response circuit coupled to the processor. See 4, component 10.

d) the fast-response circuit configurable to extract sustained evidence data from the program executing on the processor. See Fig.1, Figs.3-5, and column 2, lines 25-62. Essentially, data/error information is extracted by components 13 and 1c.

e) wherein the data path is constructed to both 1) transfer the extracted sustained evidence data to an off-chip location; and 2) to transfer the results data from the processor to an off-chip location. See Fig.4, for instance. The extracted data is sent off-chip to dive 10 via the data path. And, result data from the processor is sent off-chip to the data memory 4c via the data-path. Note that the memory is outside of the CPU so it is likely off-chip cache, RAM, or disk, all of which are off-chip.

13. Referring to claim 2, Takahashi has taught the debugging system according to claim 1, wherein:

a) the fast-response circuit is configurable to monitor program execution for a predetermined event without interfering with the program executing on the processor. See column 2, lines 40-44. When an error occurs, a visual indication is given to a debugger. Providing a visual

indication of error does not interfere with program execution. Clearly, it is configured to monitor for errors.

d) the fast-response circuit is constructed to provide an action signal responsive to the event. See column 2, lines 25-62, and column 4, line 52, to column 5, line 16. Essentially, after an error occurs, the fast-response circuit provides a signal to extract data from component 4.

14. Referring to claim 3, Takahashi has taught the debugging system according to claim 1, wherein:

a) the fast-response circuit has a first portion that is configurable to monitor the program executing on the processor for a predetermined event, and is constructed to provide an action signal upon the occurrence of the predetermined event. See column 2, lines 40-62. When an error occurs, a visual indication is given to a debugger. Providing a visual indication of error does not interfere with program execution. Clearly, it is configured to monitor for errors. Once, the error occurs, a read signal is provided to the circuit.

b) the fast response circuit has a second portion that is responsive to the action signal, and is configurable to selectively extract sustained evidence data from the program executing on the processor. See column 2, lines 25-62, and column 4, line 52, to column 5, line 16. In response to the read signal, the circuit extracts evidence data from component 4

e) the data path constructed is constructed to transfer the extracted sustained evidence data to an evidence file without interfering with the program executing on the processor. The reading of data does not interfere with the CPU because the reading makes use of components external to the CPU. See Figs.1 and 4.

15. Referring to claim 4, Takahashi has taught the debugging system of claim 1, wherein the fast-response circuit is constructed to extract the evidence data from as a commit buffer, a reorder buffer, a high-speed data bus, or a register. See Fig.4, and note data is extracted from register 4g and register 22 and from the data bus (long vertical bus in controller 20.

16. Referring to claim 6, Takahashi has taught the debugging system of claim 1, wherein the fast response circuit comprises high-speed registers. Processor 1b, which is part of the fast-response circuit, inherently includes registers. Also, component 13 includes registers to store received data for editing purposes.

17. Referring to claim 7, Takahashi has taught the debugging system of claim 1, wherein the data path comprises one or more resources of the processor's hierarchy and use of the data path is shared by both 1) results data and 2) evidence data. See Fig.4. Result data is sent, via data path, to result memory 4c. And, evidence data is sent, via data path, to debugger 10 through the interfaces.

18. Referring to claim 8, Takahashi has taught the debugging system of claim 1, wherein:

a) sequential logic is connected to the fast response circuit. See column 2, lines 20-62. The lamp-controlling circuitry and the circuitry to initiate debugging/reading by the debugger 10 is the sequential logic.

b) the sequential logic is programmable to monitor program execution for a predetermined event, and the sequential logic enables an action responsive to the program events. See column 2, lines 20-62. In response to overflow, for instance, a debugging/reading action is initiated.

19. Referring to claim 9, Takahashi has taught the debugging system of claim 1, wherein:

a) sequential logic is connected to the fast response circuit. See Fig.4. Note that processor 1b may be considered the sequential logic coupled to the fast response circuit (at least some other part of the debug system)

b) the sequential logic is programmable to selectively extract data. See column 2, lines 20-62. The processor 1b initiates debugging and extraction of data.

20. Referring to claim 10, Takahashi has taught the debugging system according to claim 8 or 9, wherein the sequential logic is constructed as a co-processor. See Fig.4, component 1b. This processor is a coprocessor with respect to processor 4a.

21. Referring to claim 19, Takahashi has taught a debugging system, comprising:

a) a processor constructed to execute a program and to generate execution results data. See Fig.4, component 4a. Processors inherently execute programs to generate results.

b) a high-speed data transfer path that is constructed to transfer execution results data, and is in communication with an external data transfer bus and file. See Fig.4 and note the data path coupling the processor 4a to components 4c-e, 4g-h, and 21-23. This data path carries result data from the processor to data memory 4c. Also, from column 2, lines 20-62, the path is in communication with an external bus in component 10 and file 13 and/or 1c.

c) a reporter circuit comprising a fast-response circuit coupled to the high-speed data transfer bus and coupled to the processor. See 4, component 10.

d) the fast response circuit configurable to extract sustained evidence data from the program executing on the processor in response to detecting a predefined event. See column 2, lines 20-62. In response to overflow, error/data information is extracted. See Figs.3 and 5.

e) a scribed constructed to transfer the extracted sustained evidence data through the high-speed

data path to an evidence file. See the abstract and column 2, lines 20-62. Extracted data is held so that it can be edited and output to a display. Therefore, the data must be stored in a file in component 13, which receives the data.

22. Referring to claim 20, Takahashi has taught the debugging system according to claim 19, wherein the high speed data path further includes one or more resources of the processor's hierarchy. Since the bus communicates with data memory (Fig.4), and the memory is a hierarchy resource, then the bus is also a hierarchy resource.

23. Referring to claim 21, Takahashi has taught the debugging system according to claim 19, wherein the fast response circuit is constructed to extract the sustained evidence data without interfering with execution of the program on the processor. The reading of data does not interfere with the CPU because the reading makes use of components external to the CPU. See Figs.1 and 4. Also, from the "summary of invention" section of Takahashi, the goal is to not interfere with, i.e., cause suspension of, the process during error handling.

24. Referring to claim 22, Takahashi has taught the debugging system according to claim 19, wherein the high-speed data path is constructed to transfer the sustained evidence data to the evidence file without interfering with execution of the program on the processor. The reading of data does not interfere with the CPU because the reading makes use of components external to the CPU. See Figs.1 and 4. Also, from the "summary of invention" section of Takahashi, the goal is to not interfere with, i.e., cause suspension of, the process during error handling.

25. Referring to claim 25, Takahashi has taught the debugging system according to claim 1, wherein program execution results are substantially unchanged whether or not the fast-response circuit extracts evidence data from execution of a given program. See Fig.4 and the "summary

of invention" section. The goal of Takahashi is to not interfere with (suspend) the processor during error data collection. Hence, results of the program execution are unchanged.

26. Referring to claim 26, Takahashi has taught the debugging system according to claim 1, wherein program execution and evidence transfer occurs substantially simultaneously. See Fig.4 and the "summary of invention" section. The goal of Takahashi is to not interfere with (suspend) the processor during error data collection. Hence, execution and error data collection occur at the same time.

27. Referring to claim 27, Takahashi has taught the debugging system according to claim 1, wherein program execution with evidence extraction and transfer occurs with a time distortion ratio that is less than 3X. See Fig.4 and the "summary of invention" section. The goal of Takahashi is to not interfere with (suspend) the processor during error data collection. Hence, there is no time distortion, where 0 is less than 3X.

28. Referring to claim 28, Takahashi has taught the debugging system according to claim 1, wherein the off-chip location is a data file. See Fig.4, component 13. This file is off processor 4a's chip. Also, note that it stores information for editing and display. Hence, the data is part of a file.

29. Referring to claim 29, Takahashi has taught the debugging system of claim 1 wherein the data path includes a communication link. This is inherent. A data path is a communication link. The data path communicates data between at least two linked components.

30. Referring to claim 30, Takahashi has taught the debugging system of claim 7 wherein resources of the processors hierarchy includes a data path associated with the processor's

hierarchy. Since the data path communicates with data memory (Fig.4), and the memory is a hierarchy resource, then the bus is also a hierarchy resource.

31. Referring to claim 31, Takahashi has taught the debugging system of claim 7 wherein resources of the processors hierarchy includes a memory associated with the processors hierarchy. See Fig.4.

Claim Rejections - 35 USC § 103

32. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

33. Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi in view of the examiner's taking of Official Notice.

34. Referring to claim 5, Takahashi has taught the debugging system of claim 1. Takahashi has not taught that the fast response circuit is integrated on-chip with the processor. However, Official Notice is taken that integrating components on a single integrated circuit is well known and accepted in the art. It is advantageous at least for the reason that it allows for lower latency communication between components because communication doesn't have to occur over multiple chips. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Takahashi such that at least part of component 10 of Fig.4 is on the same chip as processor 4a. Also, recall that integration of parts is not patentable. See *In re Larson 144 USPQ 347 (CCPA 1965).*

35. Referring to claim 11, Takahashi has taught the debugging system according to claim 8 or 9. Takahashi has not taught that the sequential logic is integrated on-chip with the processor. However, Official Notice is taken that integrating components on a single integrated circuit is well known and accepted in the art. It is advantageous at least for the reason that it allows for lower latency communication between components because communication doesn't have to occur over multiple chips. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Takahashi such that the sequential logic of Fig.4 is on the same chip as processor 4a. Also, recall that integration of parts is not patentable. See *In re Larson 144 USPQ 347 (CCPA 1965).*

36. Claims 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi in view of Roy et al., U.S. Patent Application Publication No. US 2002/0013893 A1 (herein referred to as Roy).

37. Referring to claim 23, Takahashi has taught the debugging system according to claim 1. Takahashi has not taught that the fast-response circuit is constructed to test for or to extract a branch destination from the program execution. However, Roy has taught extracting branch destination information. See TABLE 4 in paragraph [0032]. This is the information captured for purposes of debugging, and one of the items captured is the program counter (PC) value, which indicates a branch destination address when a branch occurs (note that branches occur based on paragraphs [0026]-[0027]). Clearly, the more information captured, the more a debugger can gather about execution to make an educated decision about what is occurring at run-time. As a result, in order to provide more information to a debugger, it would have been obvious to one of

ordinary skill in the art at the time of the invention to modify Takahashi such that the fast-response circuit is constructed to test for or to extract a branch destination from the program execution.

38. Referring to claim 24, Takahashi has taught the debugging system according to claim 1. Takahashi has not taught that the fast-response circuit is constructed to test for or to extract a time stamp from the program executing on the processor. However, Roy has taught extracting time stamp information. See TABLE 4 in paragraph [0032]. This is the information captured for purposes of debugging, and one of the items captured is the time stamp, which indicates when a particular instruction/event occurs. Clearly, timing information is useful to a debugger because it indicates what happens when, and the more information provided, the more of an educated decision the debugger can make about what is occurring at run-time. As a result, in order to provide more information to a debugger, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Takahashi such that the fast-response circuit is constructed to test for or to extract a time stamp from the program executing on the processor.

Response to Arguments

39. Applicant's arguments filed on May 20, 2010, have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

40. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the

patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Floyd et al., U.S. Patent No. 6,745,321, has taught harvesting problematic code sections that cause hardware hangs, and performing a subsequent recovery.

Jaggar et al., U.S. Patent No. 6,446,221, has taught a debug coprocessor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID J. HUISMAN whose telephone number is (571)272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David J. Huisman/
Primary Examiner, Art Unit 2183